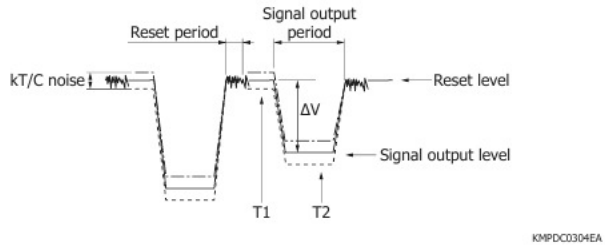
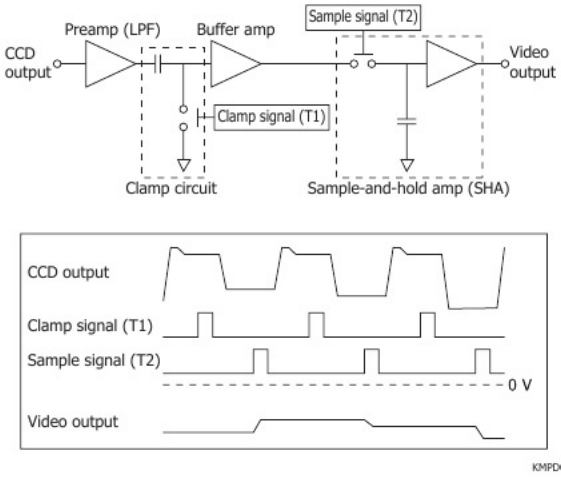
acquiring data at times T1 and T2 on the output waveform and then obtaining the difference between them will extract only a signal component ΔV with the kT/C noise removed. DC components such as the offset voltage component and reset feed-through are removed at the same time.

[Figure 1-61] CCD output waveform



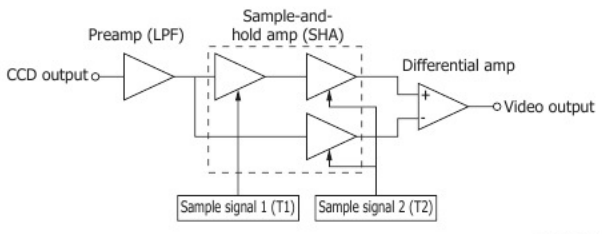
There are two types of CDS circuits: "Type 1" that uses a clamp circuit in combination with a sample-and-hold amplifier (SHA), and "Type 2" that uses a SHA in combination with a differential amplifier. Type 1 has a very simple circuit configuration [Figure 1-62]. But if the ON resistance of the switch used in the clamp circuit is large, the amount of noise that can be removed will be small or a DC voltage error will occur. Ideally, the ON resistance should be 0 Ω.

[Figure 1-62] CDS circuit block diagram (using clamp circuit and SHA)



Type 2 [Figure 1-63] uses a larger number of components but removes noise more effectively than Type 1. However, since Type 2 makes an analog calculation of the SHA output, the noise of the SHA itself may be added, resulting in increased noise in some cases. The SHA noise should be small enough so that the kT/C noise can be ignored.

[Figure 1-63] CDS circuit block diagram (using SHA and differential amplifier)



A circuit example of Type 1 is shown in Figure 1-64.
The preamp gain should be set high in order to sufficiently amplify the CCD output signal. Since the CCD output signal contains DC voltage components, a capacitor is used for AC coupling. Note that this capacitor can cause a DC voltage error if the preamp bias current is large. Therefore, a preamp with a small bias current must be selected. A JFET or CMOS input amplifier is generally used. It is also necessary to select a low-noise amplifier with a bandwidth wide enough to amplify the CCD output waveform.
The clamp circuit is made up of capacitors and an analog switch. For the analog switch, we recommend using a high-speed type having low ON resistance and small charge injection amount.
For the preamp, the last-stage amplifier is AC-coupled via a capacitor, so a JFET or CMOS input amplifier should be selected. In addition, a non-inverted amplifier must be configured to allow high input impedance.
Incidentally the CCD provides a negative-going output while the last-stage amplifier gives a positive-going output to facilitate analog-to-digital conversion. For this reason, an inverted amplifier is connected after the preamp.

High-speed signal processing circuit

For a CCD signal processing circuit that requires high-speed readout at several megahertz or faster, it is difficult for a circuit constructed only of discrete components to achieve high-speed clamp operation and fast capacitor charging/discharging response.
A high-speed signal processing circuit can be constructed by using an analog front-end IC (a single IC chip consisting of CDS, gain, and offset circuits, A/D converter, etc.) optimized for CCD signal processing.

Measures against light emission on the output circuit

If the operating conditions are not suitable for the CCD output circuit employing a two-stage MOSFET source follower, the amplifier may emit light. If this light is received by the resistive gate, storage gate, or horizontal shift register, the output for the first pixel that is read out will be large even in a dark state [Figure 1-67].
To reduce this effect, the following measure is effective.

① Apply +1 V typ. to the Vret terminal (if a Vret terminal is available).

② Intersect the horizontal shift register clock pulse (P1H, P2H) at the amplitude of 50% ± 10% [Figure 1-68].
· Horizontal 2-phase drive: P1H, P2H
· Horizontal 4-phase drive: P1H, P3H and P2H, P4H

③ After reading out all pixels, perform horizontal dummy readout up to immediately before TG is set to high level.